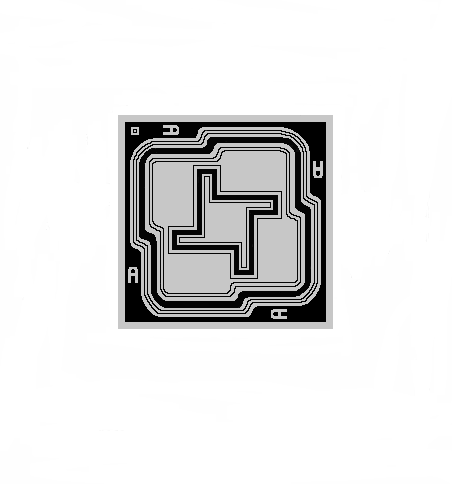
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**B**

**B**

**B**

**B**

**E**

**.023”**

**.023”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .004” X .004” B = .004” X .006”**

**Backside Potential: COLLECTOR**

**Mask Ref: BAA**

**APPROVED BY: DK DIE SIZE .023” X .023” DATE: 10/4/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 2N3117**

**DG 10.1.2**

#### Rev B, 7/19/02